Design Assignment 4 – Timers & Interrupts

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ELC 411 - Embedded Systems

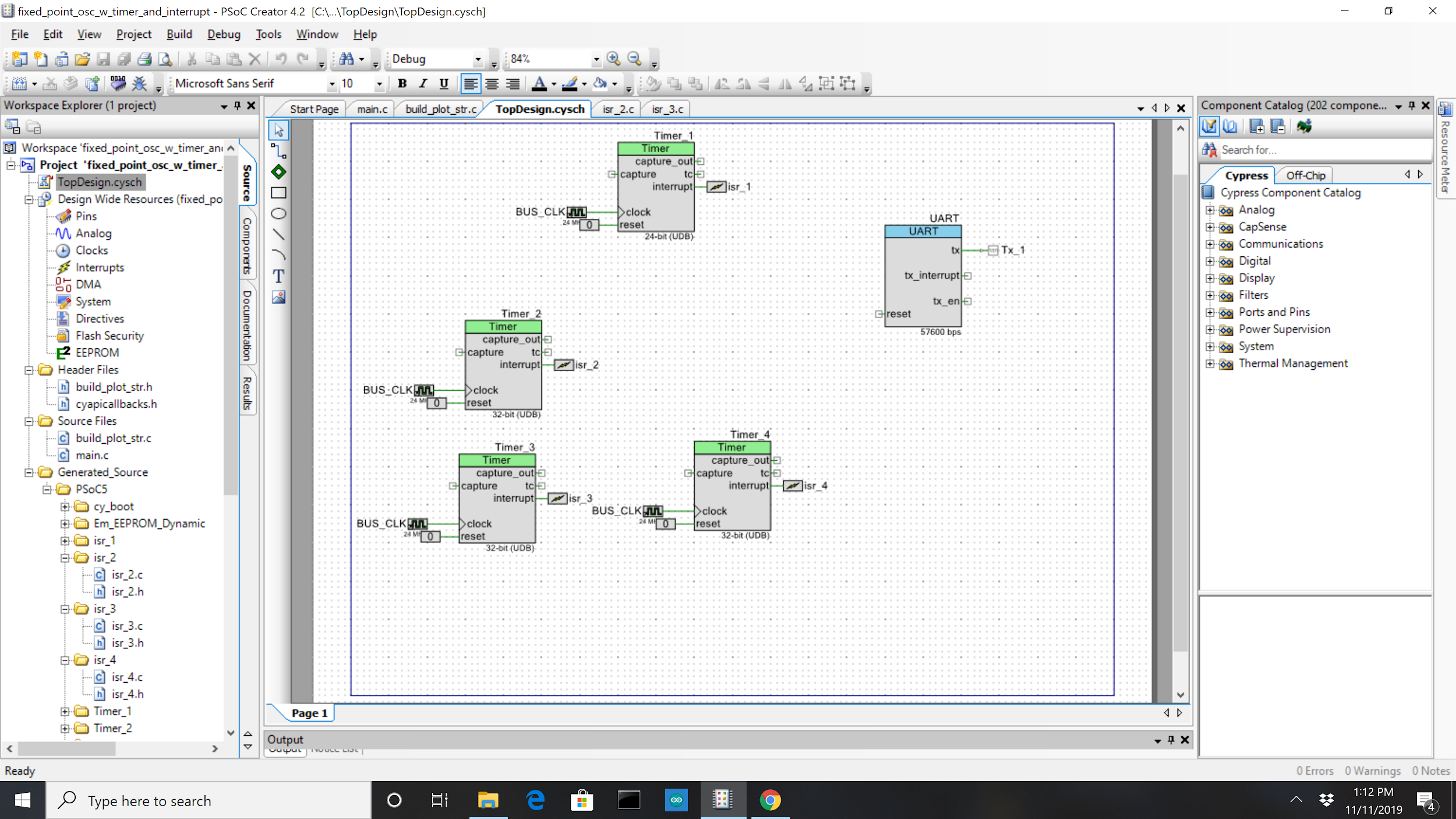
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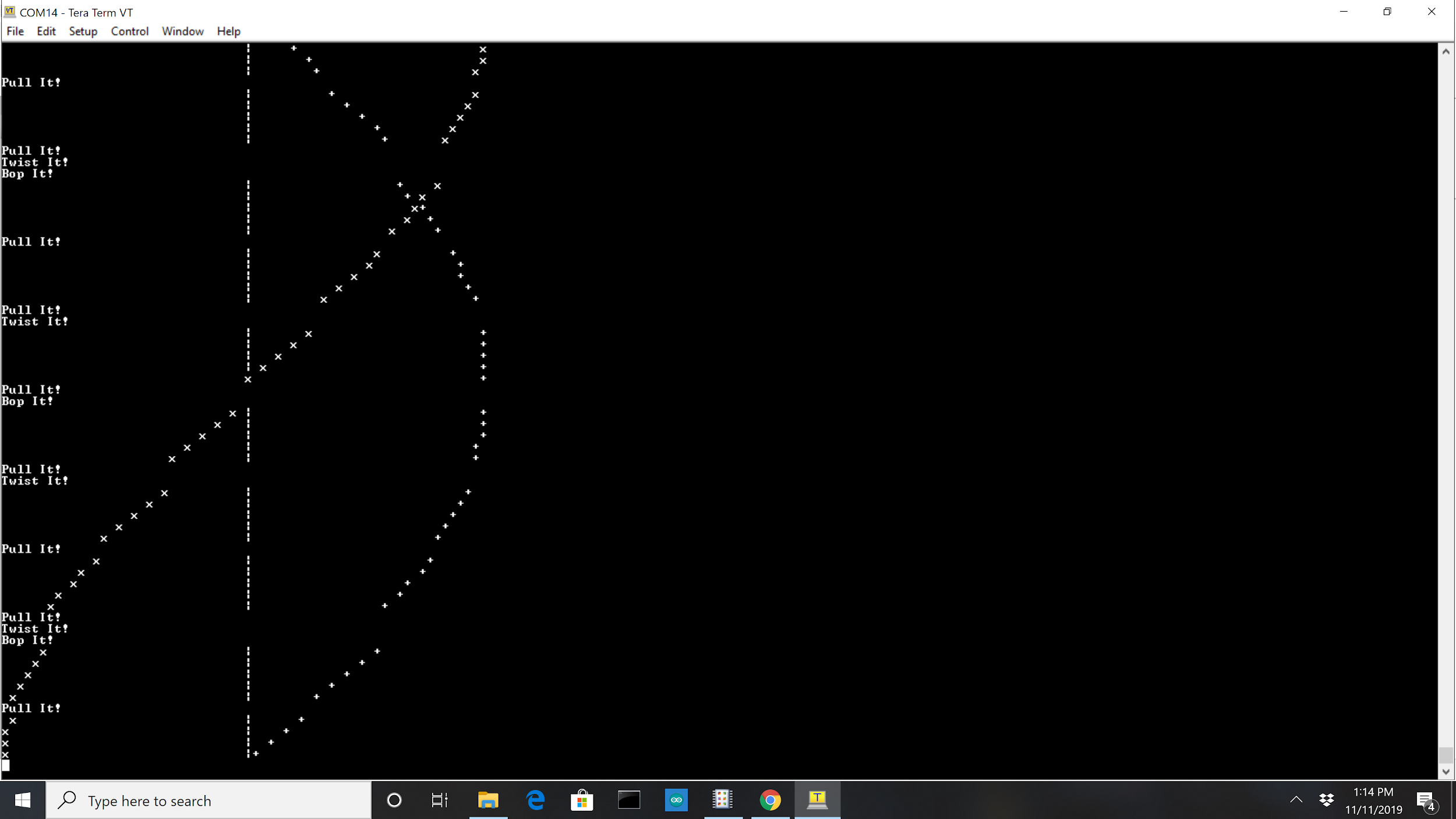
**Date Submitted: 11/15/19**

1. **Screenshot of PSoC Schematic**

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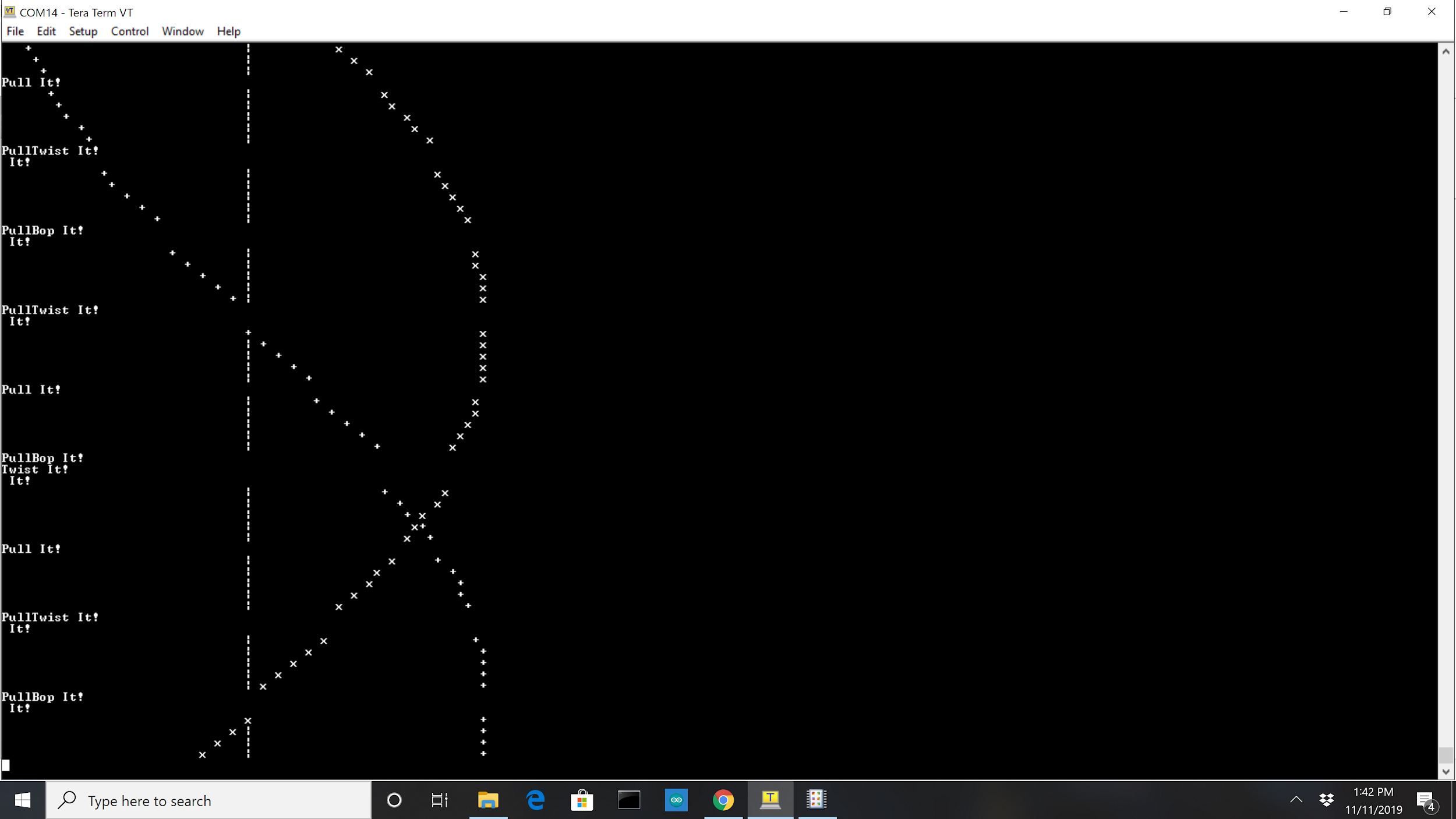
*Figure 1: PSoC Schematic*

1. **Screenshot of Tera Term At Section 3**

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*Figure 2: Tera Term Window Based on Section 3*

1. **Screenshot of Tera Term At Section 5**

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*Figure 3: Tera Term Window Based on Section 5*

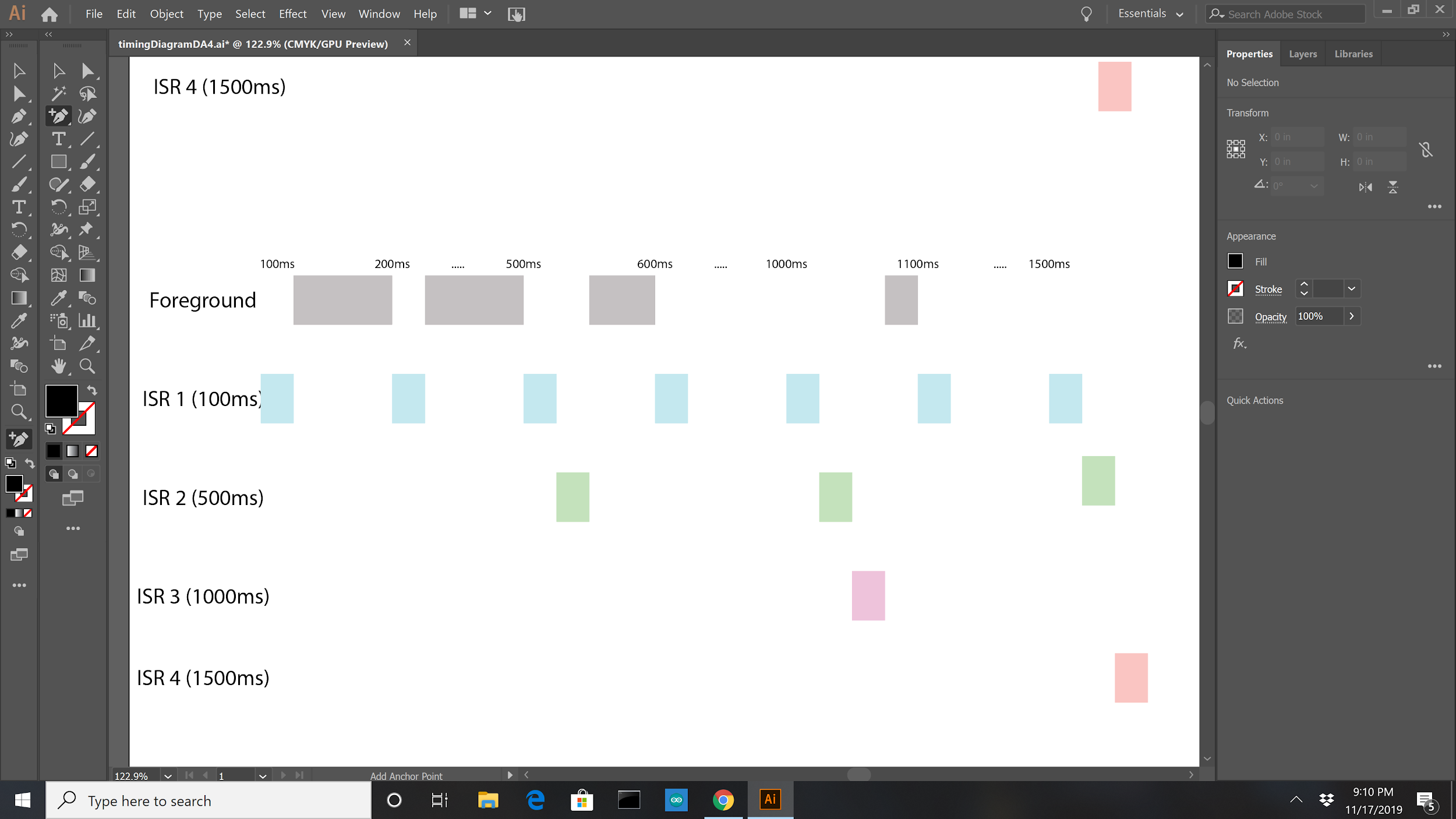
1. **Explanation of Results**

For section 3, all of the interrupts have the same priority; they executed when called and when one interrupt finished, the next one will start. The interrupts took priority over the text-based graph of the sine and cosine waves; the interrupts would break the output of the graph. For section 5 the priorities of interrupt changed. The ISR printing “Bop it” has the highest priority, followed by “Twist It”, then “Pull it” and finally the oscillator. For the result, it can be seen that interrupts are occuring in the middle of another interrupt being executed. For example at the bottom of Figure 2, the text printed it :

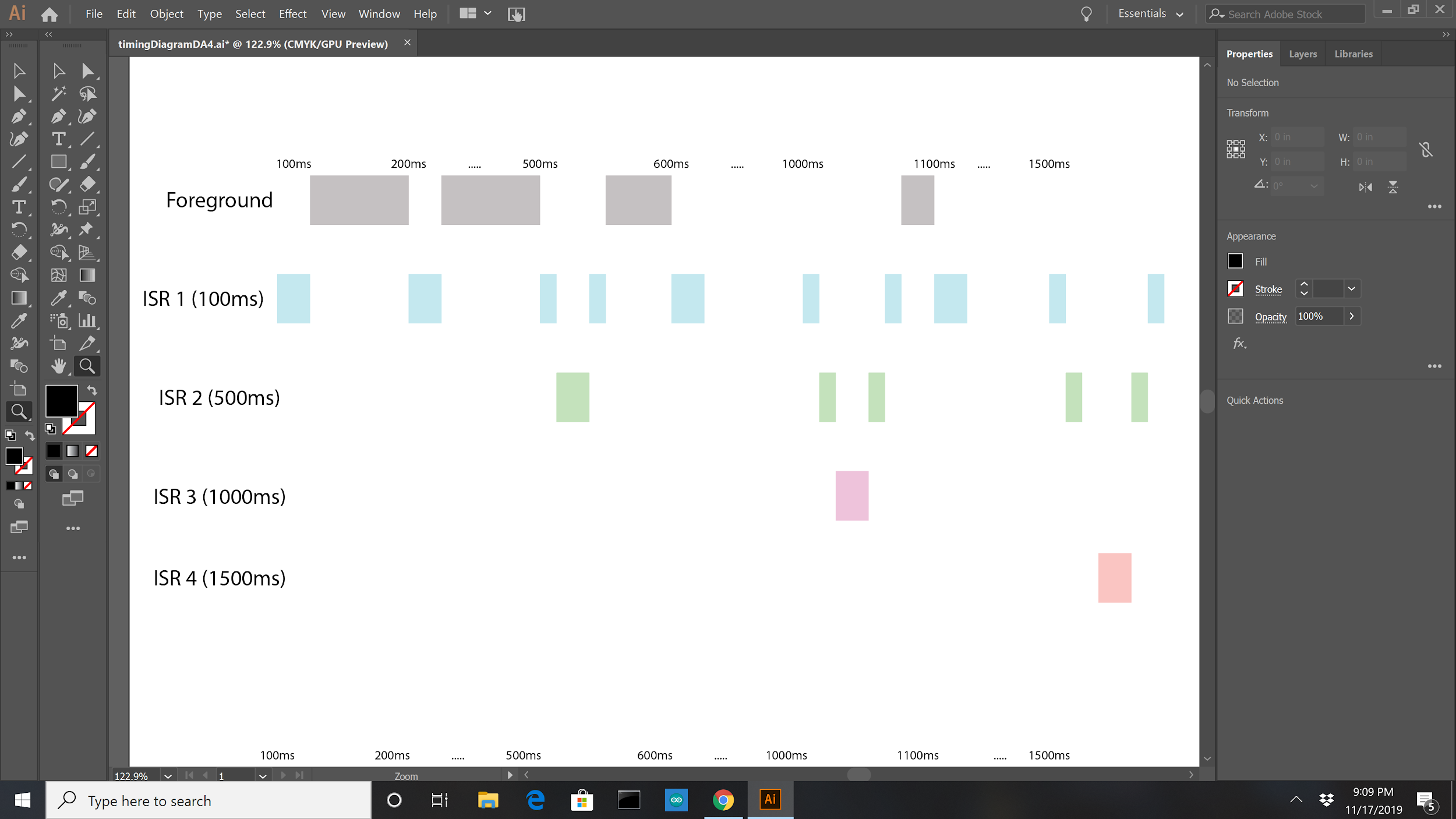
PullBop It!

It! \_\_\_\_

In the middle of printing the string “Pull It,” (ISR 2) an interrupt with higher priority is called. This is a good example of how the priority of the interrupt can affect which one occurs when. Figure 5 provides a good visual representation of how an interrupt can itself be interrupted by one of a higher priority.



*Figure 4: Timing Diagram for With all the Same Interrupt Priorities*



*Figure 5: Timing Diagram for With Adjusted Interrupt Priorities*